ABSTRACT OF THE DISCLOSURE

A memory system system includes a single in-line memory module (SIMM) which contains a memory device and a signal transmission line connected between the memory device and a connection terminal, and a dual inline memory module (DIMM) which contains two memory devices and a signal transmission line connected between the two memory devices and a connection terminal. A length of the signal transmission line of the SIMM is longer than a length of the signal transmission line of the DIMM. The load of the memory device of the SIMM is less than the load of memory devices of the DIMM, and the longer length of the signal transmission line of the SIMM increases a signal delay time of the SIMM to compensate for the different loads of the SIMM and DIMM memory devices. The longer length of the signal transmission line of the SIMM may further compensate for a signal transmission line connected between the first and second sockets which receive the SIMM and DIMM, respectively.

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